IN THE CLAIMS:

Please amend claims 1, 10, 11, 14, 15, 24, 25, 31, 38, 39 and 40 and add new Claims 43 and 44 as follows.

1. (Currently Amended) A demodulator for demodulating digital data, comprising:

a receiver circuit for receiving a transmitted digital data signal;

a correlator to correlate the digital data signal received from said receiver circuit with a reference training sequence to produce a correlation value;

a verification unit to select correlation values above a threshold value;

a determining device to determine if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing and to calculate ~~the~~ a required fractional sample delay to improve synchronization;

an implementing device implementing the calculated fractional sample delay if said determining device determines that a fractional sample delay would improve the demodulation synchronization timing; and

a demodulating device for demodulating the digital data signal.

2. (Original) A demodulator for demodulating digital data according to Claim 1, wherein said determining device comprises an algorithm that determines if a fractional sample delay would improve the demodulation synchronization timing.

3. (Original) A demodulator for demodulating digital data according to Claim 2, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine if a fractional sample delay would improve the demodulation synchronization timing.

4. (Original) A demodulator for demodulating digital data according to Claim 3, wherein the algorithm further comprises comparing first and last correlation values of the correlation curve that exceed a threshold value.

5. (Original) A demodulator for demodulating digital data according to Claim 3, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed a threshold value.

6. (Previously Presented) A demodulator for demodulating digital data according to Claim 4, wherein said determining device determines the required fractional sample delay based on the selected correlation values.

7. (Previously Presented) A demodulator for demodulating digital data according to Claim 5, wherein said determining device determines the required fractional sample delay based on the selected correlation values.

8. (Original) A demodulator for demodulating digital data according to Claim 1, wherein the fractional sample delay is in the range of −0.5 to 0.5.

9. (Original) A demodulator for demodulating digital data according to Claim 8, wherein the fractional sample delay is selected from the group consisting of ± ¼ and ½.

10. (Currently Amended) A ~~system~~ demodulator for demodulating digital data according to Claim 1, wherein said implementing device comprises an interpolation filter that implements the fractional sample delay.

11. (Currently Amended) A demodulator for demodulating digital data according to Claim 10, wherein the interpolation filter ~~comprises the steps of~~ includes (i) a multiplier for multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values, and (ii) an adder/summer for summing the fractional values.

12. (Original) A demodulator for demodulating digital data according to Claim 11, wherein said implementing device uses respective coefficients of 0.5 and 0.5 to implement a fractional sample delay of ½ sample.

13. (Original) A demodulator for demodulating digital data according to Claim 11, wherein said implementing device uses respective coefficients of 1.0 and 0.0 to implement a fractional sample delay of 0 samples.

14. (Currently Amended) A demodulator for demodulating digital data according to Claim 1, wherein said demodulator comprises ~~the~~ a demodulator portion of a VHF Digital Link Mode 2 receiver.

15. (Currently Amended) A method for demodulating digital data, comprising the steps of:

receiving a digital data signal;

correlating the received digital data signal with a reference training sequence to produce a correlation value;

selecting correlation values above a threshold value;

determining if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing and calculating ~~the~~ a required fractional sample delay to improve synchronization;

implementing the fractional sample delay if it is determined in said determining step that a fractional sample delay would improve the demodulation synchronization timing; and

demodulating the digital data signal.

16. (Original) A method for demodulating digital data according to Claim 15, wherein said determining step comprises an algorithm that determines if a fractional sample delay would improve the demodulation synchronization timing.

17. (Original) A method for demodulating digital data according to Claim 16, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine in said determining step if a fractional sample delay would improve the demodulation synchronization timing.

18. (Original) A method for demodulating digital data according to Claim 17, wherein the algorithm further comprises comparing first and last correlation values of the correlation curve that exceed a threshold value.

19. (Original) A method for demodulating digital data according to Claim 17, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed a threshold value.

20. (Currently Amended) A method for demodulating digital data according to Claim 18, wherein said determining step further ~~comprises determining an amount of~~ determines the required fractional sample delay ~~necessary to improve the demodulation synchronization timing~~ based on the selected correlation values.

21. (Currently Amended) A method for demodulating digital data according to Claim 19, wherein said determining step further ~~comprises determining an amount of~~ determines the required fractional sample delay ~~necessary to improve the demodulation synchronization timing~~ based on the selected correlation values.

22. (Original) A method for demodulating digital data according to Claim 15, wherein the fractional sample delay is in the range of −0.5 to 0.5.

23. (Original) A method for demodulating digital data according to Claim 22, wherein the fractional sample delay is selected from the group consisting of ± ¼ and ½.

24. (Currently Amended) A method for demodulating digital data according to Claim 15, wherein said implementing step ~~comprises~~ includes an interpolation step using an interpolation filter ~~that implements~~ to implement the fractional sample delay.

25. (Currently Amended) A method for demodulating digital data according to Claim 24, wherein the interpolation ~~filter~~ step comprises the steps of (i) providing input samples and multiplying first and second samples of each pair of the input samples by respective coefficients to obtain two fractional values, and (ii) summing the fractional values.

26. (Original) A method for demodulating digital data according to Claim 25, wherein a fractional sample delay of 0 samples is implemented in said implementing step by using respective coefficients of 1.0 and 0.0.

27. (Original) A method for demodulating digital data according to Claim 25, wherein a fractional sample delay of ½ sample is implemented in said implementing step by using respective coefficients of 0.5 and 0.5.

28. (Previously Presented) A method for demodulating digital data according to Claim 15, wherein a VHF Digital Link Mode 2 radio receiver is provided for implementing the method.

29. (Original) A method for demodulating digital data according to Claim 15, wherein a digital circuit is provided for implementing the method.

30. (Original) A method for demodulating digital data according to Claim 15, wherein a process is provided for implementing the method.

31. (Currently Amended) Computer executable code for implementing a method for demodulating digital data, said code for executing the steps comprising:

receiving a digital data signal;

correlating the received digital data signal with a reference training sequence to produce a correlation value;

selecting correlation values above a threshold value;

determining if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing and calculating ~~the~~ a required fractional sample delay to improve synchronization;

implementing the fractional sample delay if it is determined in said determining step that a fractional sample delay would improve the demodulation synchronization timing; and

demodulating the digital data signal.

32. (Original) Computer executable code for implementing a method for demodulating digital data according to Claim 31, wherein said determining step comprises an algorithm that determines if a fractional sample delay would improve the demodulation synchronization timing.

33. (Original) Computer executable code for implementing a method for demodulating digital data according to Claim 32, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine in said determining step if a fractional sample delay would improve the demodulation synchronization timing.

34. (Original) Computer executable code for implementing a method for demodulating digital data according to Claim 33, wherein the algorithm further comprises comparing first and last correlation values of the correlation curve that exceed a threshold value.

35. (Original) Computer executable code for implementing a method for demodulating digital data according to Claim 33, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed a threshold value.

36. (Previously Presented) Computer executable code for implementing a method for demodulating digital data according to Claim 34, wherein said determining step further determines the required fractional sample delay based on the selected correlation values.

37. (Previously Presented) Computer executable code for implementing a method for demodulating digital data according to Claim 35, wherein said determining step further determines the required fractional sample delay based on the selected correlation values.

38. (Currently Amended) Computer executable code for implementing a method for demodulating digital data according to Claim 31, wherein said implementing step ~~comprises~~ includes an interpolation step using an interpolation filter ~~that implements~~ to implement the fractional sample delay.

39. (Currently Amended) Computer executable code for implementing a method for demodulating digital data according to Claim 38, wherein the interpolation ~~filter~~ step comprises the steps of (i) multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values, and (ii) summing the fractional values.

40. (Currently Amended) Computer executable code according to Claim ~~30~~ 31, wherein a computer readable medium is provided for storing computer executable code.

41. (Previously Presented) A method for demodulating digital data, comprising the steps of:

receiving a digital data signal;

correlating the received digital data signal with a reference training sequence to produce a correlation value;

selecting correlation values above a threshold value;

determining an amount of fractional sample delay to be added to a demodulator's symbol sampling timing based on the selected correlation values;

implementing the fractional sample delay; and

demodulating the digital data signal.

42. (Previously Presented) A demodulator for demodulating digital data, comprising:

receiving means for receiving a digital data signal;

correlating means for correlating the digital data signal received from said receiving means with a reference training sequence to produce a correlation value;

verification means to select correlation values above a threshold value;

determining means for determining an amount of a fractional sample delay to be added to a demodulator's symbol sampling timing based on the selected correlation values;

implementing means for implementing the fractional sample delay; and

demodulating means for demodulating the digital data signal.

43. (New) A modulator for demodulating digital data according to Claim 1, wherein said correlator receives the reference training sequence at the beginning of each transmission.

44. (New) A modulator for demodulating digital data according to Claim 43, wherein the reference training sequence identifies the transmitted digital data signal as a VDL Mode 2 signal.